Associate Professor	Department of Electrical and Computer Engineering and Space Systems Academic Group (1996-present). *Teach graduate courses in Electrical and Computer Engineering and Space Systems Engineering: Si VLSI Design, Advanced Si VLSI and Gallium Arsenide (GaAs) Digital IC Design, Fault Tolerant Computing, Microprocessors for Space Applications, Microprocessor Based Systems Design, Computer Architecture, Advanced Computer Architecture and Parallel Processing, Logic Design and Switching Theory, Analog and Digital Circuits, and others. Supervise student research, theses, and dissertations on topics such as high-speed/low-power GaAs and InP logic circuits, the effects of radiation on GaAs and Si digital ICs, VLSI and GaAs IC and system-on –a-chip design, fault-tolerant microprocessor systems for space applications, etc.*
Assistant Professor	Department of Electrical and Computer Engineering and Space Systems Academic Group (September 1990-June 1996).
Co-Principal Investigator	Department of Electrical and Computer (October 2000-September 2003). Contract: Digital Target Imaging Architecture for Multiple Large Target Generation. Sponsor: Office of Naval Research and Naval Research Laboratory. *Development of equations and algorithms necessary to digitally synthesize false radar return images in electronic attack systems to counter wideband imaging radars. Development of a system-level architecture, a microarchitecture, and a system-on-a-chip implementation for use in the U.S. Navy Advanced Integrated Electronic Warfare System.*
Principal Investigator	Space Systems Academic Group and Department of Electrical and Computer Engineering (May 199-April 2000). Contract: CEPXS/SPICE Automated Software Interface Development. Sponsor: Lockheed Martin Space and Missile Systems. *Development of an automated software interface between CEPXS (Coupled Electron/Proton Transport Simulator) and SPICE (Simulation Program with Integrated Circuit Emphasis) to allow accurate simulation of the operation of microelectronic circuits while exposed to nuclear radiation.*
Co-Principal Investigator	Space Systems Academic Group and Department of Electrical and Computer Engineering (October 1995-September 1998). Contract: Radiation-Immune, High-Speed, Low-Power, Gallium Arsenide, Digital Integrated Circuits. Sponsor: National Security Agency/U.S. Navy - Space and Naval Warfare Systems Command/U.S. Naval Research Laboratory. *Theoretical and laboratory investigation of the effects of buried, low-temperature grown buffer layers on the single event upset sensitivity of gallium arsenide integrated circuits. Development of high-speed, low-power, radiation-immune, GaAs ICs using substrates with buried, low-temperature grown, buffer layers.*
Principal Investigator	Space Systems Academic Group and Department of Electrical and Computer Engineering (October 1996-September 1998). Contract: Radiation Tolerant Bulk CMOS Digital Integrated Circuits. Sponsor: National Security Agency. *Experimental investigation of circuit and mask layout techniques for producing radiation-tolerant digital ICs using commercial bulk CMOS fabrication processes.*

Principal Investigator	Department of Electrical and Computer Engineering (October 1997-September 1998). Contract: Tactor Interface and Controller Design for the Tactile Situational Awareness System. Sponsor: Naval Aerospace Medical Research Laboratory. *Development of a single-chip VLSI tactor interface and microcontroller for interfacing to and controlling a tactile situational awareness system.*
Principal Investigator	Department of Electrical and Computer Engineering (October 1996-Septeber 1997). Contract: Dynamic Logic Circuits for Complimentary GaAs Fabrication Processes. Sponsor: National Security Agency. *Simulation and experimental investigation of low-power, high-speed, dynamic logic circuits for use with complementary GaAs fabrication processes.*
Principal	Department of Electrical and Computer Engineering (October 1995-September 1997). Contract: Read Prediction Cache Memories for Embedded Microprocessor Systems. Sponsor: U.S. Navy – Space and Naval Warfare Systems Command. *Theoretical and simulation investigation of data cache miss address prediction methods. Development of alternatives to off-chip, second-level, cache memories for spacecraft, weapon system, and other embedded high-performance microprocessor applications.*
Principal Investigator	Space Systems Academic Group and Department of Electrical and Computer Engineering (October 1995-September 1996). Contract: Evaluation of CAD/CAM Software Tools for Designing Radiation-Hardened Digital Integrated Circuits. Sponsor: National Security Agency. *Investigation and evaluation of commercial CAD/CAM software tools for use in designing space qualified digital integrated circuits using a proprietary radiation-hardened call library.*
Principal Investigator	Space Systems Academic Group and Department of Electrical and Computer Engineering (October 1992-Spetember 1995). Contract: Radiation Tolerant, High-Speed, Low-Power, Gallium Arsenide Dynamic Logic. Sponsor: U.S. Navy - Space and Naval Warfare Systems Command. *Laboratory investigation of single event upsets caused by ionizing radiation in gallium arsenide dynamic logic circuits. Development of new circuits and techniques for use in radiation-tolerant, high-speed, low-power computers and digital systems.*
Principal Investigator	Department of Electrical and Computer Engineering (October 1990-September 1992). Contract: VLSI Design Education. Sponsor: National Science Foundation. *Received funding for fabricating integrated circuits designed by students in the FLSI design courses that I taught.*
Principal Investigator	Department of Electrical and Computer Engineering (October 1990-September 1992). Contract: Design Principles for Very High-Speed Digital Circuits and Systems. Sponsor: U.S. Naval Postgraduate School, Research Initiation Program. *Initiated a new research program in gallium arsenide (GaAs) digital IC design. Research focused on the design of new, high-speed driver, receiver, and transceiver circuits for bus-connected digital systems and computers.*